DEPFET Sensor R&D and Prototyping

- Status -

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Most of the design done by Rainer Richter, MPI HLL

Two DEPFET runs for SuperBelle

First run PXD6: 2009

-: first DEPFET run on SOI wafers!!

→ 50 µm thin DEPFET arrays

-: 6 SOI and 2 std. Hi-Res Wafer

-: top wafer (front side) technology like PXD5

-: new: thinning and back side processing

-: Aim: - find optimal design

- optimize technology and yield

- provide devices for all-silicon module

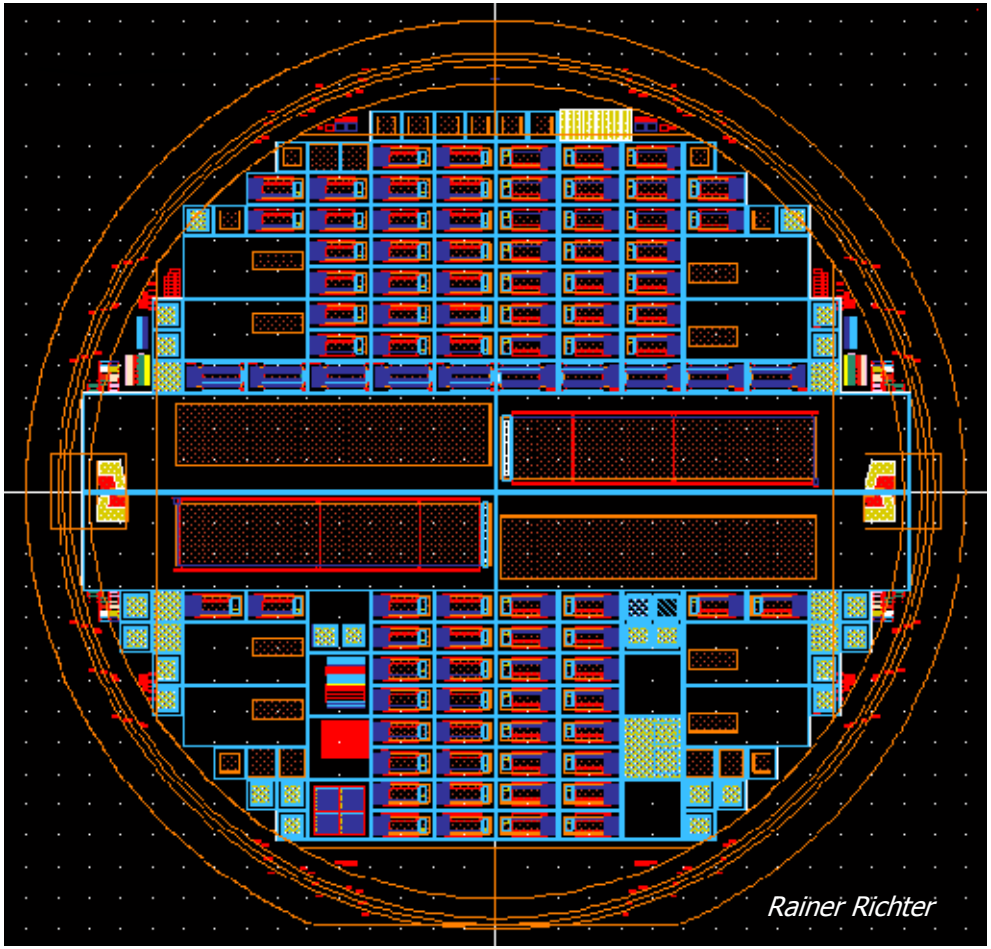
End Spring 2010

SuperBelle Production PXD7: Start 2011

-: With improved rad hard technology

-: 20 Wafer? (depends on yield of PXD6)

End Spring 2012



wafer floor plan for PXD6

Status of the Design

-: Many design variations – pixel size, geometry of the cell, matrix arrangement…

-: Wafer floor plan and size of the matrices are frozen, detailed design not yet

- deadline is middle of May, still some optimization possible (and ongoing..)
- discussion and selection process at dedicated DEPFET Workshop 2-6 May
- most important designs will be placed at the DEPFET Wiki for discussion prior to that (www.depfet.org).

-: four half sized first layer modules in the center (≈5cm^2 sensitive region) with variable pixel size along Z → all-silicon ladder with bump bonded ASICs

-: many (≈60) smaller wire-bondable matrices for laser/beam tests, irradiations etc. ..

-: 8 fully bump-bondable matrices for interconnection tests

-: ILC sensors many test structures (Diodes, MOS-Caps, MOSFETs ..)

DEPFET Pixel Cell for SuperBelle

DEPFETs from ILC to SuperKEKB:

-: the principle is of course the same

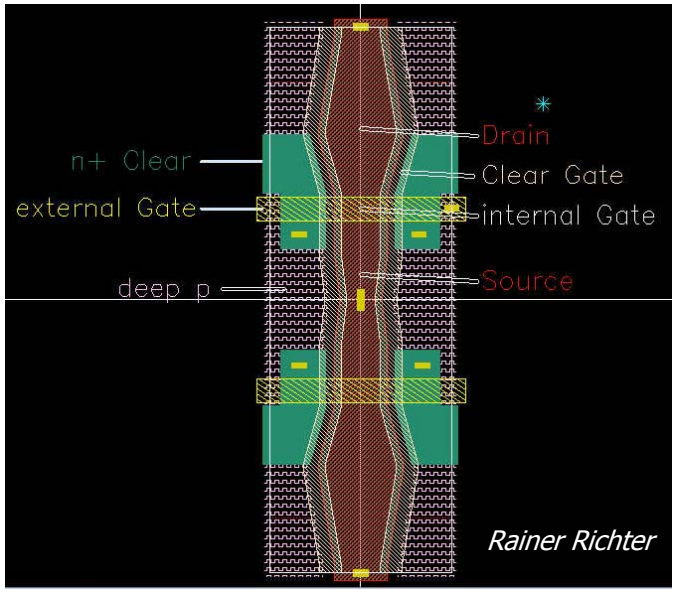
-: technology to a large extent also

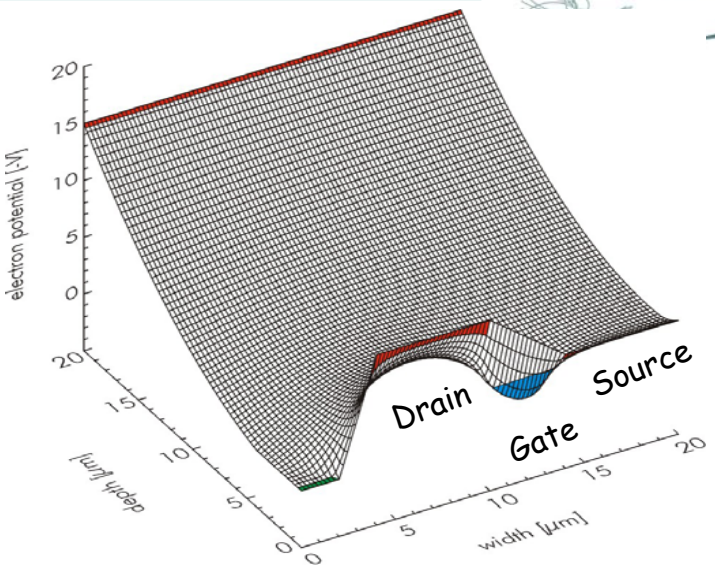
-: but the cell size is much larger!!!

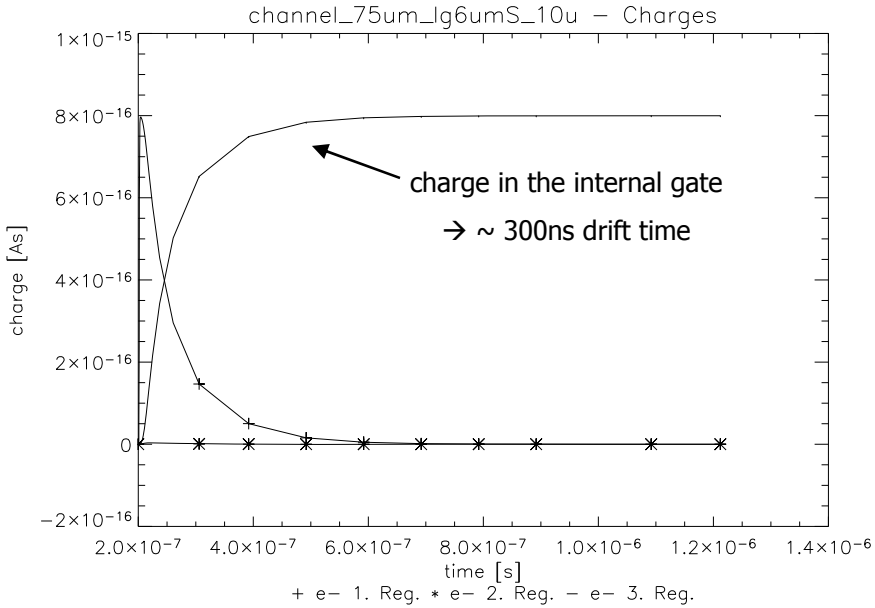
24x24μm² → 50x75μm²

→ keep W and L small (maintain clear and g_q)

→ re-design drain and source region to keep charge collection time short (<<10μs)







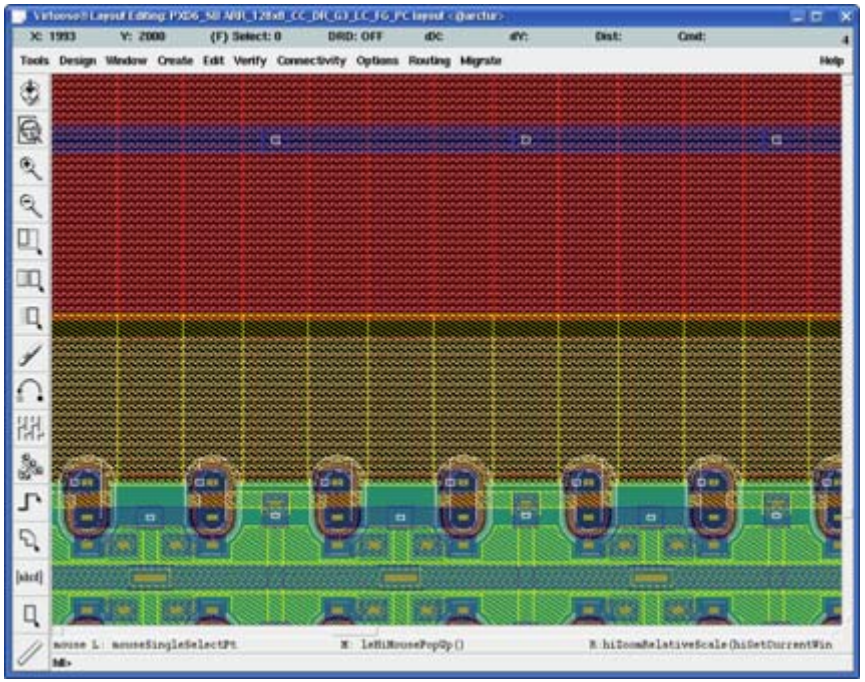
Beyond 120 µm long pixel….

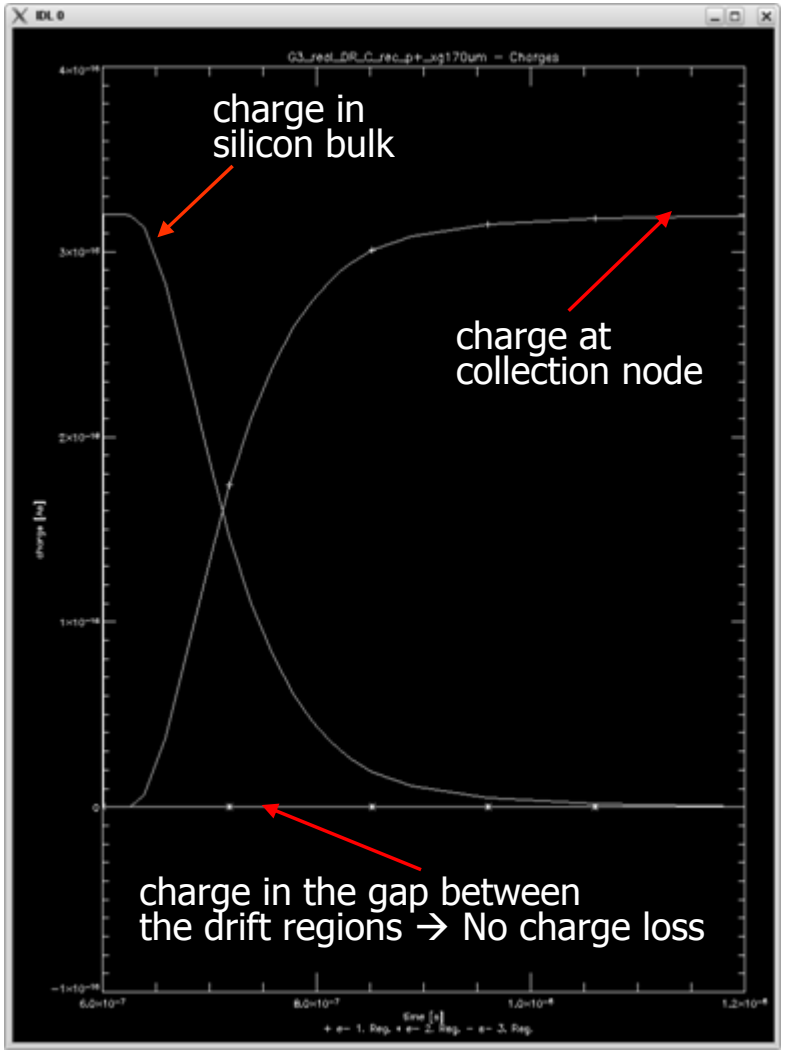
-: add drift structures to guide signal charge into the internal gate

-: 220 µm pixel (in z) possible with two drift regions

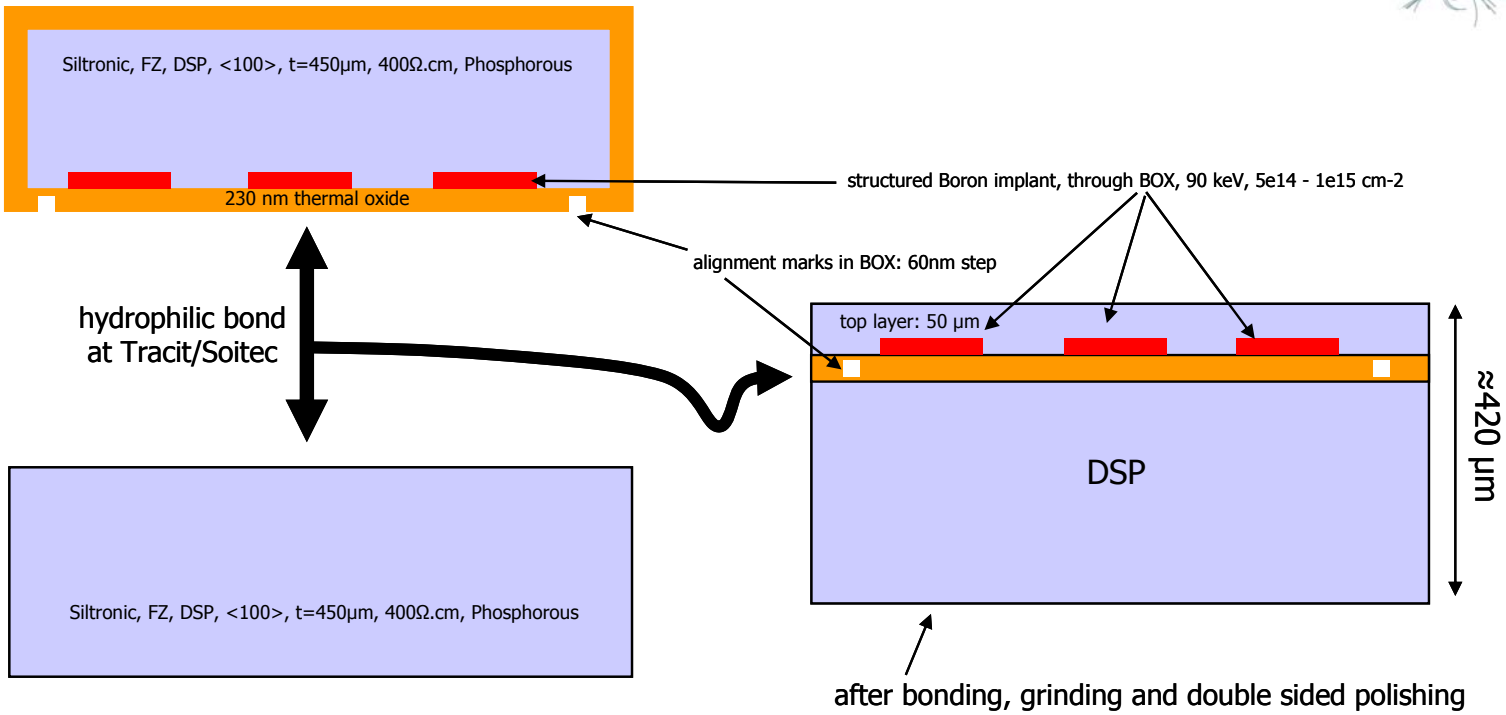
→ drift time ≈250 ns for 90% of the charge

for the most extreme case





Production Status PXD6



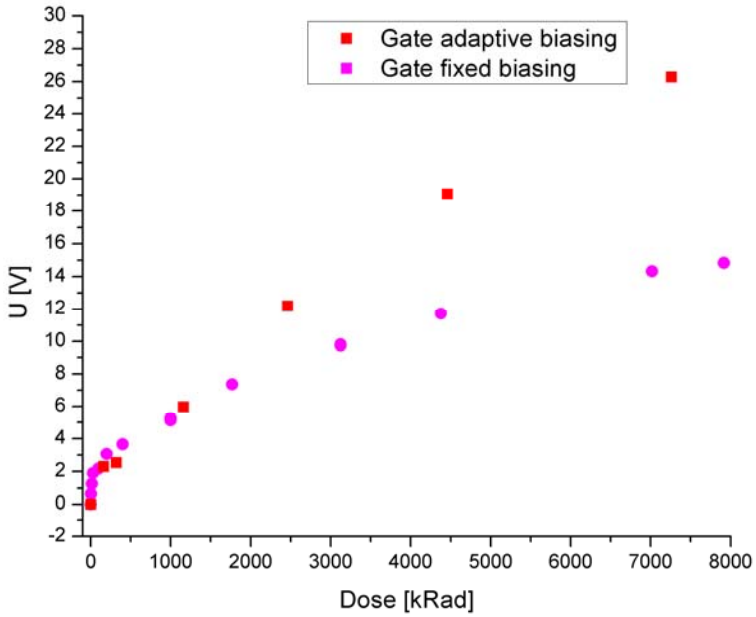
-: Preparation of Wafers for SOI production finished

- oxidation, alignment marks etching, implantation, cleaning etc. → Done!

-: Send out wafers to Tracit for Wafer bonding and top layer thinning next week

confirmed delivery date: **22.05.09**

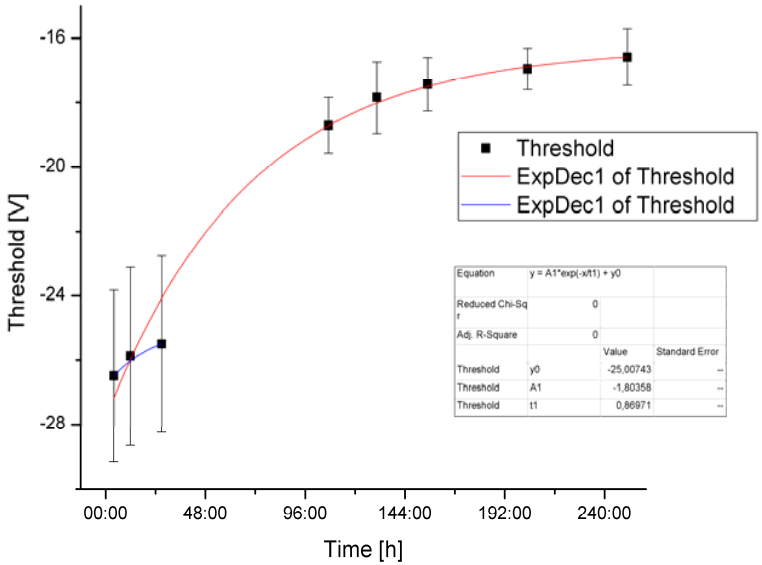
The Radiation Tolerance Issue



-: PXD5, Wafer 90, 8x12 mini-matrix, 32x24 μm^2
-: irradiation with X-rays photons in Karlsruhe, ~185krad/h, Emax=60keV
-: entire matrix biased in "off" during irradiation, periodically cleared

a/ "gate off" voltage and common clear gate voltage was stepwise adapted to radiation induced threshold voltage shift

b/ "gate off" voltage kept at 0V all the time



-: Threshold voltage shift depends on biasing condition during irradiation up to 8Mrad

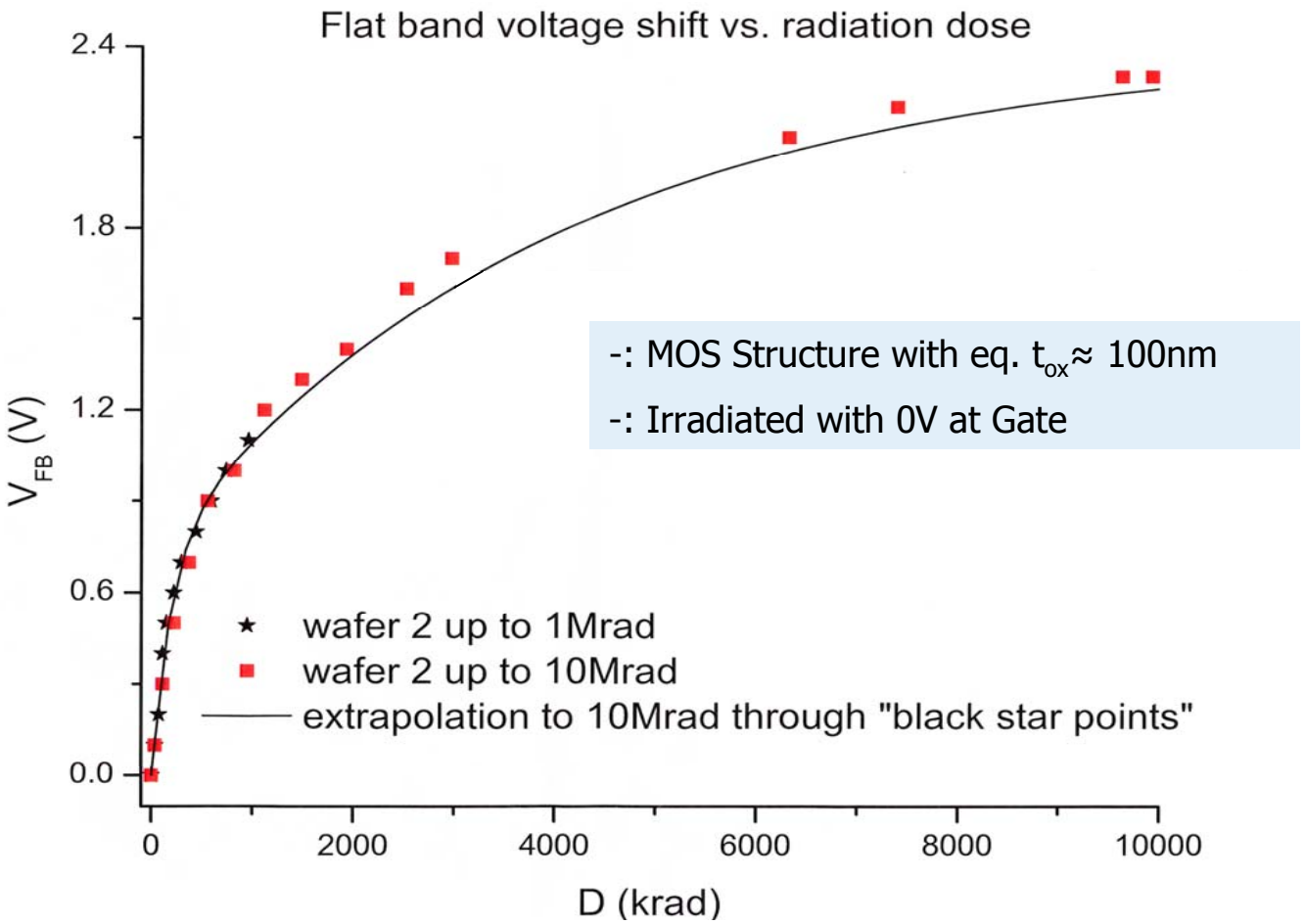
-: For negative Vgate during irrad. worse behavior

-: Annealing at RT (10 days) → ΔVt≈16.5 +/- 0.8 V

-: noise and signal okay even after 8Mrad!

only Gate shown here; Clear Gate behaves similar!

Consequences : Improve Technology → better Gate Dielectric



→ Smaller (simpler) DEPFET technology test run planned in parallel to PXD6 production

→ **DEPFETs with thinner and optimized gate dielectrics in the final run!**

Summary

-: PXD6 Production has started and is on schedule!

-: Detailed design is being finalized, geometry will be frozen beginning/middle of May

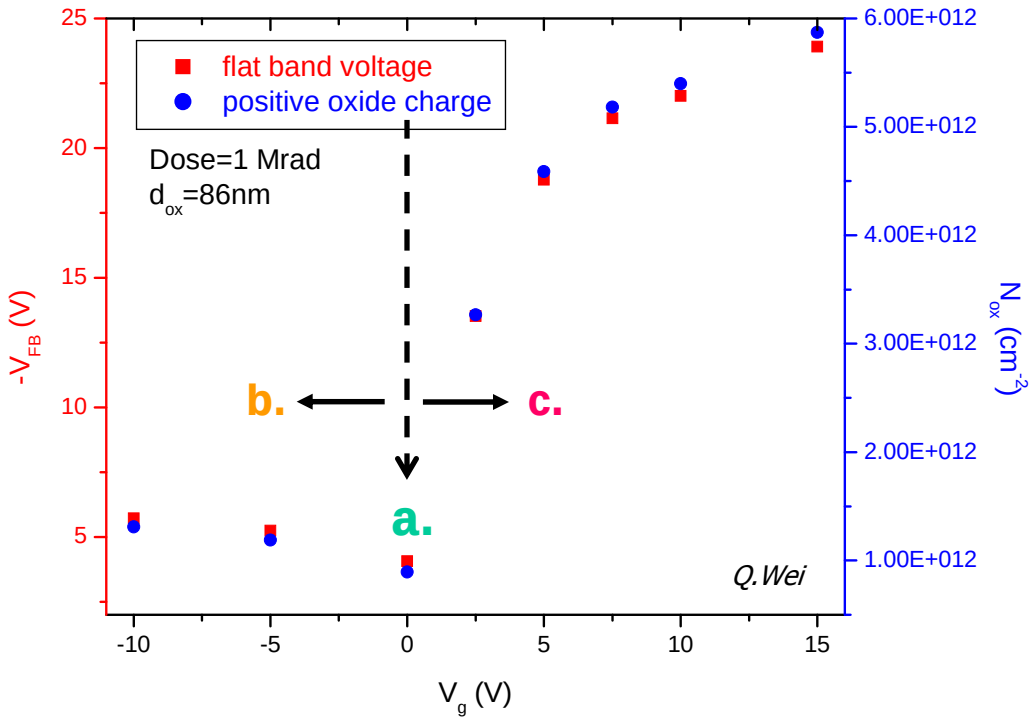
-: New irradiation results of MOS-Caps with improved gate dielectrics show very encouraging results. This technology will be further optimized in a parallel production run and integrated in the DEPFET technology for the final SuperBelle sensor.

DEPFET Workshop at Ringberg Castle, 3-6 May 2009

http://indico.mppmu.mpg.de/indico/conferenceDisplay.py?confId=466

- Backup slides follow

Reasons II - Field Dependence, MOS-C irradiations



Region a.:

Field minimal, DEPFET in "OFF" state, no channel, region under gate depleted and floating

Region b.:

small negative voltage at gate, DEPFET "ON", charges in SiO2 separated → higher charge yield

Region c.:

positive voltage on gate, e- drift do poly gate, holes trapped at interface, not possible in DEPFET!

But "channel" close to the Source is not completely floating!!

→ adaption of Gate-off voltage to negative values during irradiation increases the field there

→ Gate "OFF" close to the Source is then in Region b.

→ larger threshold voltage shift, if one tries to keep ($V_{Gate\text{-}On}$-$V_{Gate\text{-}Off}$) constant in the experiment